Amendments to the Specification:

Please replace the paragraph beginning at page 1, line 10, with the following paragraphs:

This application is a continuation of U.S. Application Serial No.09/878,984, filed June 11, 2001, and entitled "Multiprocessor Cache Coherence System And Method In Which Processor Nodes And Input/Output Nodes Are Equal Participants."

This application is related to, and hereby incorporates by reference, the following U.S. patent applications:

- Scalable Multiprocessor System And Cache Coherence Method, filed June 11, 2001, Serial No. 09/878,982~~attorney docket number 9772-0326-999~~.
- System And method for Daisy Chaining Cache Invalidation Requests In A Shared-Memory Multiprocessor System, filed June 11, 2001, Serial No. 09/878,985~~attorney docket number 9772-0329-999~~.
- Cache Coherence Protocol Engine And Method For Processing Memory Transaction In Distinct Address Subsets During Interleaved Time Periods In A Multiprocessor System, filed June 11, 2001, Serial No. 09/878,983~~attorney docket number 9772-0327-999~~.

Please replace the paragraph beginning on page 2, line 19 with the amended paragraph below.

In summary, a computer system has a plurality of processor nodes and a plurality of input/output nodes. Each processor node includes ~~a~~ one or more processor cores, an interface to a local memory ~~system~~subsystem and a protocol engine implementing a predefined cache coherence protocol. Each processor core has an associated memory cache for caching memory lines of information. Each input/output node includes no processor cores, an input/output interface for interfacing to an input/output bus or input/output device, a memory cache for caching memory lines of information and an interface to a local memory subsystem. The local memory subsystem of each processor node and input/output node stores a multiplicity of memory lines of information. The

protocol engine of each processor node and input/output node implements the same predefined cache coherence protocol.

Please replace the paragraph beginning on page 6, line 1 with the amended paragraph below.

Each processor core (PC) 106 is directly connected to dedicated instruction cache (iL1) 108 and data cache (dL1) 110 modules. These first-level caches (L1 cache modules) 108, 110 interface to other modules through an intra-chip switch (ICS) 112. Also connected to the ICS 112 is a logically shared second level cache (L2) 114 that is interleaved into eight separate modules 116, each with its own controller, on-chip tag, and data storage. Coupled to each L2 cache 116 is a memory controller (MC) 118 that preferably interfaces directly to a memory bank of DRAM (dynamic random access memory) chips (not shown) in a memory subsystem 123. In a preferred embodiment, each memory bank provides a bandwidth of 1.6_GB/sec, leading to an aggregate bandwidth of 12.8 GB/sec. Also connected to the ICS 112 are two protocol engines, the Home Protocol Engine (HPE) 122 and the Remote Protocol Engine (RPE) 124, which support shared memory across multiple nodes 102, 104 of the system. Multiple nodes are linked by a subsystem including a router (RT) 126, an input queue (IQ) 128, an output queue (OQ) 130, a packet switch (PS) 132, and a packet switched interconnect 134. The router ~~136~~126 sends and receives packets to and from other nodes via the interconnect 134. The interconnect 134 physically links multiple nodes 102, 104. In a preferred embodiment, the total interconnect bandwidth (in/out) for each node is 32 GB/sec. Finally, a system control (SC) module 136 takes care of miscellaneous maintenance-related functions (e.g., system configuration, initialization, interrupt distribution, exception handling, performance monitoring).